Remarks:

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Status of Claims

Claims 1 – 3, 6 – 8, 10, 12, 19 – 23, 27, 28, 30, 32 and 39 – 54 are pending in the application. Claims 1 – 3, 6 – 8, 10, 12, 19 – 23, 27, 28, 30, 32 and 39 – 54 have been rejected.

Claims 1, 7, 8, 45, 51 and 54 have been amended. No new matter has been added.

35 U.S.C. 112, first paragraph Rejections

The Office Action rejects claims 45 – 54 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, for using the terms "B-bit" and "B" which are not found in the specifications as originally filed. Applicants respectfully traverse the rejection, in view of the remarks that follow.

Independent claims 45 and 51 as amended recite "B is the logarithm to base 2 of the number of states in a stage" and independent claim 54 as amended recites "B is the logarithm to base 2 of the number of said states". Therefore, "B" is fully defined in claims 45 – 54. "B" is merely a symbol that represents a number, the number being defined as above. Similarly, "B-bit" is clearly understood to be that number of bits.

As explained in the "Background of the Invention" of the specification, the most common binary convolution codes have 2^{K-1} states, where the constraint length K is for example, 5, 6, 7 or 9. For such codes, B = K-1. In general $B = \log_2 N$, where "N" represents the number of states. In the case of FIGS. 14 and 15A – 15D, where the trace bits of a stage are stored in a single memory cell, B = L, where L is the integer part of the logarithm to base 2 of the number of states stored in the memory cell (the "length of the memory cell"). In the case of FIGS. 16A – 16C, where the trace bits of a stage are stored in P memory cells, then B = L + P – 1, where L is defined as above, and P is the number of memory cells.

In other words, although the symbol "B" has not been used explicitly in the specification as originally filed, "B" is related by simple mathematical relationships to the symbols "K", "N", "P" and "L", which are found in the specification as filed. Therefore, claims 45 – 54 are fully supported by the specification as filed.

35 U.S.C. 112, second paragraph Rejections

The Office Action rejects claim 7 under 35 U.S.C. 112, second paragraph, as being indefinite for reciting "said at least one arithmetic logic unit" when claim 1 recites "no more than one arithmetic logic unit". Claim 7 has been amended to recite "said arithmetic logic unit", thus overcoming the rejection.

35 U.S.C. 102 Rejections

The Office Action rejects claims 8, 10, 12, 19 – 23, 27, 28, 30, 32 and 39 – 54 under 35 U.S.C. 102(e) as being anticipated by US 5,987,490 (Alidina et al.). Applicants respectfully traverse the rejection, in view of the remarks that follow.

As is well established, in order to successfully assert a *prima facie* case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (MPEP 2131)

Claims 44 - 50

The Final Office Action states "Regarding claim 44, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits."

Applicants strongly disagree with this statement. As explained in the instant application at page 4, line 1 – page 5, line 5, "for each source symbol received, there is a transition between states ... The trace bit associated with the transition is determined during the "select" step of the "add-compare-select" operation when calculating the weights." "...

the trace bits are used to trace back the optimal path from a "final" state to an "original" state, the path and the original state enabling reconstruction of the transmitted data. ... one can wait until all of the transmitted symbols have been received in order to begin the traceback ... an alternative method is to begin the decoding procedure when the memory is full".

Applicants wish to point out that the Viterbi algorithm has two separate processes involving trace bits. The first process is to generate the trace bits as part of the output of the add-compare-select (ACS) operation. Indeed, each trace bit is an indication of which state was selected in the "select" portion of the add-compare-select operation. Alidina et al. teaches "a dual-MAC processor optimized so that two Viterbi ACS operations, including traceback bit storage, can be executed in two machine cycles". This process of generating the trace bits and storing them in registers is illustrated, by way of example, in FIGS. 5A – 5C and FIGS. 6 – 7 of the instant application. The second process is to trace back the optimal path from a "final" state to an "original" state, the optimal path and the original state enabling reconstruction of the transmitted data.

While the abstract of Alidina et al. states that "two Viterbi ACS operations, including traceback bit storage, can be executed in two machine cycles", no mention is made whatsoever of the number of machine cycles required in the Viterbi traceback routine. **Indeed, Alidina et al. is silent as to any features of the Viterbi traceback routine,** other than to state "The third step is known as traceback. This step traces the maximum likelihood path through a trellis of possible present state to next state transitions ... and reconstructs the path through the trellis to extract the original input data" (col. 2, lines 48 – 53).

Therefore, the Final Office Action's statement "Each clock cycle will trace back a number of bits" is unsupported and probably incorrect.

Alidina et al. does not disclose, either expressly or inherently, *"tracing back, stage by stage, in as few as two clock cycles per stage, states of binary convolution codes that are decoded using Viterbi decoding"*, as recited by claim 44. Therefore Alidina et al. cannot anticipate claim 44 and its dependent claims 45 – 50.

Alidina et al. does not disclose, either expressly or inherently, the following limitation of claim 45: *"generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits*

equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state ... wherein B is the logarithm to base 2 of the number of states in a stage".

Claims 51 – 53 and 54

The Final Office Action states "Regarding claims 51, 52 and 54, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits."

Applicants strongly disagree with this statement. While the abstract of Alidina et al. states that "two Viterbi ACS operations, including traceback bit storage, can be executed in two machine cycles", no mention is made whatsoever of the number of machine cycles required in the Viterbi traceback routine. **Indeed, Alidina et al. is silent as to any features of the Viterbi traceback routine.** Therefore, the Final Office Action's statement "Each clock cycle will trace back a number of bits" is unsupported and probably incorrect.

Alidina et al. does not disclose, either expressly or inherently, the following limitation of claim 51: *"generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state ... wherein B is the logarithm to base 2 of the number of states in a stage".* Therefore Alidina et al. cannot anticipate claim 51 and its dependent claims 52 – 53.

Alidina et al. does not disclose, either expressly or inherently, the following limitation of claim 54: *"a memory element to store in its B least significant bits a B-bit binary representation of an index of a state of a stage, where B is the logarithm to base 2 of the number of said states".* Therefore Alidina et al. cannot anticipate claim 54.

Claims 8, 10 and 12

Claim 8 recites *"a storage device having memory cells, wherein a group of at least one memory cell is to store all trace bits for a stage of Viterbi decoding of a binary convolution code in sequential order, another group of at least one memory cell is to store all trace bits for a subsequent stage of Viterbi decoding of said binary convolution code in sequential order, and yet another group of at least one memory cell is to store all trace bits*

for a further subsequent stage of Viterbi decoding of said binary convolution code in sequential order".

Fig. 2 of Alidina et al. illustrates a Viterbi algorithm butterfly computation for a 16-state convolution code. Therefore, in each stage of the Viterbi algorithm, 16 trace bits are calculated, one for each state: "Once calculation of the two path metrics for each state is completed, the values are compared and the minimum or the maximum, depending on implementation details, is selected as the survivor cost and the corresponding traceback bit (TB) is determined and stored." (col. 3, lines 4-8).

Alidina et al. discloses storing trace bits in two traceback registers 46, denoted ***ar0*** and ***ar1***. TB0 is stored in ***ar0*** and TB8 is stored in ***ar1*** (see col. 8, line 57- col. 9, line 8). According to Alidina et al., "Preferably, each traceback register 46 is 16-bits wide" (col. 5, lines 26-27). In other words, the pair of traceback registers can store at most the trace bits for two stages. The pair of traceback registers cannot simultaneously store the trace bits for more than two stages. Therefore, Alidina et al. does not teach, either explicitly or inherently, the limitations of claim 8 and consequently, Alidina et al. cannot anticipate claim 8. Claim 10 is dependent from claim 8 and includes all the limitations of the independent claim. Therefore, Alidina et al. cannot anticipate claim 10.

Claim 12 as amended recites similar limitations to those of claim 8 as well as additional limitations. Therefore Alidina et al. cannot anticipate claim 12.

Claims 19 – 23, 27 and 28

According to Alidina et al, the traceback output is shifted into two separate registers ***ar0*** and ***ar1***.

Alidina et al. does not disclose *"a storage device having memory cells, wherein for each of said multiple stages, a group of one or more memory cells is to store said trace bits in sequential order"*, as recited by claim 19. The two registers 46 shown in FIG. 3 can store trace bits of at most two stages. Therefore, the two registers 46 of Alidina et al. may be considered to be *"a first register and a second register to jointly store a single copy of trace bits of at least a portion of one stage"*, as recited by claim 19. However, the storage device recited by claim 19 is a separate component of the binary convolution decoder, apart from the first register and second register.

Therefore Alidina et al. does not disclose all the limitations of claim 19 and its dependent claims 20 – 23. Consequently, the Office Action has failed to establish a prima facie case of anticipation regarding claims 19 – 23.

Alidina et al. does not disclose *"saving said trace bits in sequential order to a group of one or more memory cells"* as recited by amended claim 27. Therefore Alidina et al. cannot anticipate claim 27 as amended. Claims 28, 30 and 32 are dependent from claim 27 and include all the limitations of the independent claim. Therefore Alidina et al. cannot anticipate claims 28, 30 and 32.

Alidina et al. does not disclose *"for each of said multiple stages, storing said trace bits in sequential order in a group of one or more memory cells"*, as recited by claim 39. Therefore Alidina et al. does not disclose all the limitations of claim 39 and its dependent claims 40 – 43. Consequently, the Office Action has failed to establish a *prima facie* case of anticipation regarding claims 39 – 43.

35 U.S.C. 103 Rejections

The Office Action rejects claims 1 – 3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over US 5,987,490 (Alidina et al.) in view of US 5,715,470 (Asano et al.). Applicants respectfully traverse the rejection, in view of the remarks that follow.

As explained hereinabove with respect to the rejections under 35 USC 102, Alidina et al. discloses a dual-MAC processor to perform two Viterbi "add-compare-select" operations, including traceback bit storage, in two machine cycles (abstract). The processor includes two adders 32, each operating in split mode for the Viterbi operation: "The two adds are performed as 16-bit split adds in one of the two adders 32 ... the two subtracts are performed as 16-bit split subtracts on the other adder 32" (col. 8, lines 37 – 42). Signals 78 output from the adders 32 are stored in two registers 46 as trace bits generated by the "add-compare-select" operation (Fig. 3). Alidina et al. is silent as to the method or mechanism by which traceback is performed using the trace bits.

In contrast, Asano et al. discloses an arithmetic apparatus for performing the traceback using trace bits (called "path select signals" in Asano et al.) once the trace bits have already been calculated for several (or all) stages. Indeed, in FIGS. 3 – 6 of Asano et al, "data memory 1 stores ... path select signals". Therefore, the ALU 8 shown in FIGS. 3, 5

and 6 of Asano et al. does not operate "to determine trace bits for Viterbi decoding of a binary convolution code".

The Examiner's proposed modification of Alidina et al. to use a single ALU instead of two would destroy the intended function of Alidina et al., namely to perform two Viterbi "add-compare-select" operations in two machine cycles. Therefore, it is unlikely that a person of ordinary skill in the art would make such a modification.

Accordingly, Alidina et al. and Asano et al., alone or in combination, fail to teach or suggest all the limitations of claim 1 as amended.

Claims 2 – 3, 6 and 7 are dependent from claim 1 and include all the limitations of the independent claim. Therefore, Alidina et al. and Asano et al., alone or in combination, fail to teach or suggest all the limitations of claims 2 – 3, 6 and 7.

Applicants therefore request that the Examiner withdraw the rejection of claims 1 – 3, 6 and 7 under 35 U.S.C. 103(a).

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,

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